Code No: D0605, D5509, D7701, D6801, D5701 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II - Semester Examinations, March/April 2011
SYSTEM ON CHIP ARCHITECTURE
(COMMON TO DIGITAL SYSTEMS & COMPUTER ELECTRONICS, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
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1. a) With a neat sketch explain ARM programming model.
   b) What do you mean by pipelining? Briefly explain about 5 stage pipeline in ARM. [12]

2. a) Explain about the structure of the ARM cross – Development tool kit.
   b) Briefly discuss about the Features of ARM which are not shared by most other RISC Architectures. [12]

3. a) Discuss the various features of FPA10.
   b) Explain the coprocessor Register transfer instructions? Why the instruction cannot used for Register transfer of CP15 coprocessor. [12]

4. What are the various signals involved in interfacing of memory with ARM? With a neat diagram how a memory is interfaced with ARM and explains it's read and write operations. [12]

5. What are the various debugging techniques? Explain the ARM debug hard ware architecture? [12]

6. a) With a neat diagram explain set associate cache and fully associative cache.
   b) What are advantages of having embedded memory on chip? How it is useful in increasing the efficiency of the system. [12]

7. a) Explain the ARM MMU architecture.
   b) How the synchronization is occurred between the various processes in ARM. Explain. [12]

8. Write short notes on the following:
   a) Context switching.
   b) Data types in ARM.
   c) Condition execution. [12]

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